Study of solar cells by using MOSFET implemented with the Diamond layout style

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***Abstract*—This work aims to perform an initial study of solar cell implemented by a planar structure based on the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) biased and implemented with the Diamond (hexagonal gate shape) layout style. The experimental data have shown that the Diamond MOSFET can be considered as an alternative base cell to be used to implement solar cells.**

Keywords— Solar cells, MOSFETs, Unconventional gate Layout Styles for MOSFETs.

I. INTRODUCTION

The solar energy is one of the fastest growing renewable sources in the world and one of the most popular. In 2016 around 350 TWh were produced in the world and this energy could represent 30% of the electricity generated in the world in 2022, according to the International Energy Agency (IEA) [1].

One of the big problems with this technology is that its efficiency is very low, resulting in an increase in the cost its implementation [2]. The most used photovoltaic cells nowadays are made of crystalline silicon [3]. They occupy a large part of the international solar energy market [3]. The great advantage of the solar cell is that it has a relatively small production cost due to the great abundance of silicon in the world. Researchers from all over the world don't measure efforts to improve the electrical performance of this devices and therefore there are a lot of researches in this engineering area, such as studies for improve the methods of the electrical energy transmission and storage, and a large part of the researches in the generation area, such as the use of new surface texturing processes of the solar cells [4], anti-reflective coating engineering [5], among others. It is known that the innovative layout styles are capable of improve the electrical performance of the MOSFETs [6],[7]. In this scenario, the motivation of this paper is to perform an initial study of solar cell implemented by a planar structure based on the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) biased and implemented with the Diamond (hexagonal gate shape) layout style focusing on improving its electrical performance [8]. This work proposes an innovative idea, there are no previous studies on this device as a solar cell.

II. LITERATURE REVIEW

A. Photoelectric effect

The photoelectric effect is based on the emission of energy packages called photons through electromagnetic radiations. The photons are particles that have an energy of their own. This energy (E) can be calculated using Equation (1) [9].

$$E = h * v \quad (1),$$

where h is the Plank constant and v is the photon frequency. The photoelectric effect usually occurs on metal plates exposed to electromagnetic radiations. When the photons strike the metal surface, they can transfer their energies to the electrons, removing them from the metal with a certain kinetic energy (KE). This only occurs when the photon has energy superior to the working function of the material (Φ) [9].

B. Typical solar cell

The solar cell is the device used to convert light energy into electrical energy through the photovoltaic effect. Today's solar cells are mostly made of crystalline silicon. These cells have an efficiency that can vary between 14% and 22%, but their production cost is relatively low. When grouped, they are called solar panel [10].

When these cells are exposed to electromagnetic radiations the photoelectric effect occurs, releasing the electrons from the material. They are captured in the form of electrical current, this is called photocurrent (I_{ph}). On the other hand, when the solar cell is not exposed to electromagnetic radiations, it does not generate any type of electrical current or voltage and works as a diode and produce an electrical current called diode current (I_D) [10]. The equivalent electrical circuit is illustrated in Figure 1 [11].

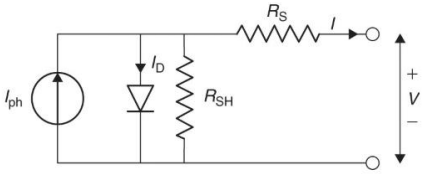

Figure 1: Electrical circuit equivalent of a solar cell [11].

In Figure 1, Iph is photocurrent, I_D is the electrical current of the diode, R_S is the series electrical resistance, which corresponds to the solar cell's internal series resistance, R_{SH} is a shunt electrical resistance and V and I are respectively, the output electrical voltage and current, generated by the solar cell. The electric current generated of the solar cell (I) can be obtained through the difference between I_{ph} and I_D to added the current that flows by the R_{SH} and V is calculated by the difference between the potential difference of the parallel connection, given by I_{ph}, the diode and R_{SH}, and the potential difference of R_S. Figure 2 shows the cross-section of a typical solar cell [11].

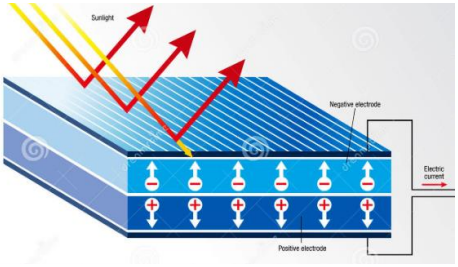

Figure 2: Cross-section of a typical solar cell [12].

C. *Metal-Oxide-Semiconductor Field Effect Transistor*

The Metal-Oxide-Semiconductor Field Effect Transistor with insulated gate, covers many applications in the electronics environment. The conventional MOSFETs have a rectangular gate geometry. Figure 3 shows the cross-section of this kind of device [13]. This device presents four terminals: the drain, gate, source and body (substrate). There are two different types of MOSFETs: channel p (pMOSFET) and channel n (nMOSFET). Besides, these devices work in different operation modes: accumulation and enhancement. In this paper we are focusing on the enhancement mode. The two types of MOSFETs follow the same operation principle, but each one has a type of doping in the channel region (pMOSFET: n type substrate and nMOSFET: p type substrate) [13].

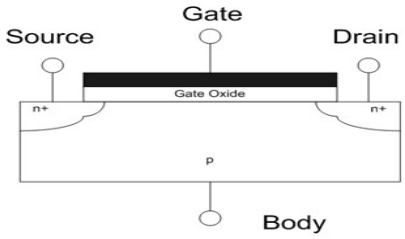

Figure 3: Example of a simplified cross-section of a conventional nMOSFET [14].

In Figure 3, n+ is the strongly doped region with pentavalent elements and p represents a weakly doped region with trivalent elements.

Between the gate and substrate regions there are a very thin layer of silicon dioxide (SiO_2), which it is an excellent insulator. To form an electrode in the gate, a metal is placed on top of this oxide, forming the gate contact. A metal is also deposited on top of the source, drain and substrate regions, establishing a contact area on top of each one of them [13].

When an external voltage is applied between the gate and source (V_{GS}), which must be bigger than the threshold voltage (V_{TN}), a channel composed of mobile charge carriers is created between the source and drain regions, and consequently generating an electrical current flow in the longitudinal direction, since there is a potential difference between drain and source regions, i.e., from drain to source regions (I_D), which is directly proportional to the ratio of the width (W) by the length (L) channel. Besides, I_D can be controlled by application of V_{GS} and V_{DS} [13]. There are three operating modes in this device: I- the cut-off mode, where there is no current flow (V_{GS} is small than V_{TN}); II- the triode mode, where it has a similar operation to a resistor (V_{GS} higher or equal to V_{TN} and V_{DS} smaller than $V_{GT}=V_{GS}-V_{TN}$, which V_{GT} is called as overdrive gate voltage); III- the saturation mode, which seems to behave as a current source (V_{GS} higher or equal to V_{TN} and V_{DS} higher or equal to V_{GT}). Figure 4 illustrates I_D as a function of V_{DS} for four different values of V_{GS} (V_{GS1}, V_{GS2}, V_{GS3}, V_{GS4}). It shows the three operating modes of nMOSFET (cut-off, triode and saturation), which $V_{DS(sat)}$ is the value of V_{DS} which the transistor operates between the triode and saturation regions [13].

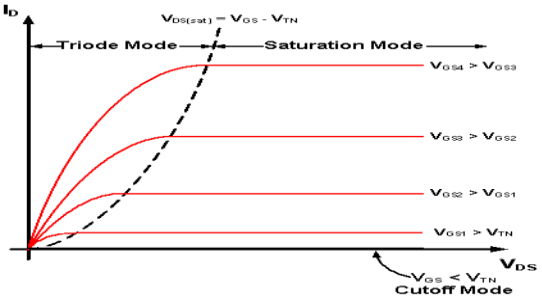

Figure 4: Characteristic curves I_D as a function of V_{DS} for different V_{GS} values [15].

Figure 5 presents the other characteristic curve of the nMOSFETs (I_D as a function of V_{GS}) regarding a V_{DS} value. Note that, as the V_{GS} is smaller than V_{TN}, I_D is practically null [13].

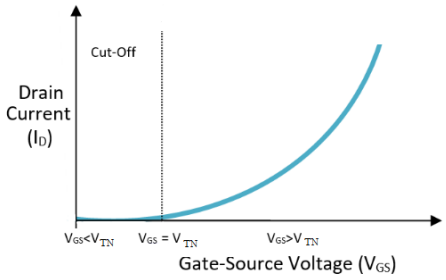

Figure 5: Characteristic curve I_D vs V_{GS} [16].

The simple mathematics model that describes nMOSFET I_D in the cut-off, triode and the saturation regions are given by Equation (2): I_D, Equation (3): I_D(lin) and Equation (4): I_D(sat), respectively [13].

$$I_D = 0 \qquad (2),$$

$$I_D(lin) = \frac{\mu_n . C_{ox}}{2} . \frac{W}{L} . [2.(V_{GS} - V_{TN}).V_{DS} - V_{DS}^2] \quad (3),$$

$$I_D(sat) = \frac{\mu_n . C_{ox}}{2} . \frac{W}{L} . (V_{GS} - V_{TN})^2 . (1 + \lambda . V_{DS}) \quad (4),$$

where μn is the mobile charge carriers in the channel, C_{ox} is the oxide capacitance per area unit and λ is MOSFET parameter [13].

D. MOS-structure solar cell

The MOS-structure solar cell consists of an n-type layer on a p-type silicon (Substrate), a thin gate oxide (SiO_2) layer, a transparent Indium Tin Oxide (ITO) gate electrode, two ohmic contacts on the drain and source regions, an electrode on the back (substrate) and an auxiliary voltage source, as shown in Figure 6 [17].

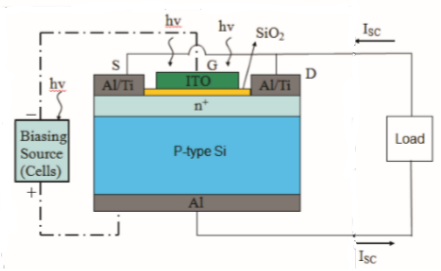

Figure 6: Example of a cross-section of a MOS-Si photovoltaic cell with the gate biased by an external voltage source and the source and drain terminals are short-circuited [17].

In Figure 6, the drain and source contacts are short-circuited and connected to a load, which in turn is connected to the substrate electrode. There is an external auxiliary voltage source connected to the gate of the MOS-structure through of its negative terminal, while its positive terminal is connected to the substrate contact. The external voltage source induces negative charges in the gate and therefore the majority carriers are repelled of the n+ region and consequently reducing the depletion region between n-type and p-type silicon placed in the substrate of the device. Therefore, this approach facilitates the flow of electrons of the n+ semiconductor to the p semiconductor and consequently increasing the value of I_{SC}, as this device is submitted the electromagnetic radiations (Figure 7). The electromagnetic radiations incidence in the device go through the gate, striking the n-type material and in some cases hitting the p-type material as well. When the photons strike in the n+ material, the electrons of the valence band can gain energy enough to pass to the conduction band, which are collected by the drain and source regions to compose the electric current (I_{SC}) [17].

In Fig. 7, V_G is the potential energy of the gate in relation the ground.

Regarding a V_G of 5V, Fig.7 shows that the I_{SC} is 12.93% higher than the one measured, as V_G is equal to 0V [17].

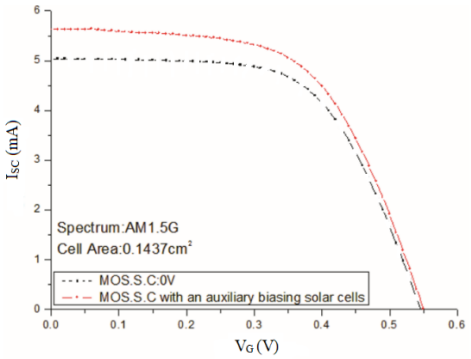

Figure 7: Photovoltaic ISC-VG characteristics of an MOS-structure solar cell measured under AM1.5G illumination and biased with an auxiliary source (Voc =5 V) [17].

E. Diamond MOSFET

The Diamond MOSFET (DM) is a transistor with a non-conventional gate geometry, that is, its gate geometry is not rectangular, that in this case it is hexagonal. Because of this change of the gate shape, this device presents the longitudinal corner effect which boost the longitudinal electric field along of channel [18]. This change enhances its electrical performance, increasing the drain current (I_{DS}), the maximum effective mobility (μ_{eff}) and the transconductance (g_m) and, in addition to reducing the on-state series resistance (R_{on}), as compared to those of the conventional rectangular MOSFET. The disadvantage of this technology is to present its off-state drain current (I_{off}, at V_{GS}=0) greater than the one of the conventional rectangular MOSFET, which increases the power consumed in the device and can limit its use in the digital applications. The structure of Diamond SOI MOSFET (DSM) is shown in Figure 8 [18].

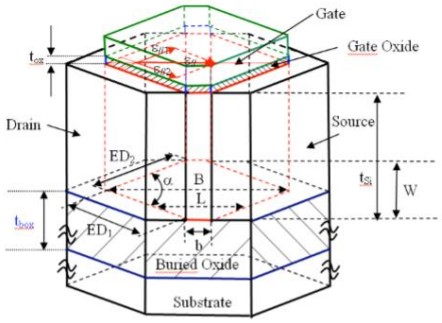

Figure 8: Diamond SOI MOSFET structure [18].

In Figure 8, t_{si}, t_{ox} and t_{box} are the silicon film, the gate-oxide and buried-oxide thickness, B and b are the largest and smallest channel lengths, respectively, and α is the angle between the sides ED1 and ED2 of the trapezoidal structure of the gate. Because of the new gate geometry of the Diamond MOSFET, three news effects are generated in its structure: The Longitudinal Corner Effect (LCE), the Parallel Connections of MOSFETs with Different Channel Lengths (PAMDLE) and the Deactivation of Parasitic MOSFTs in the Bird's Beak Regions (DEPAMBBRE) [18-19]. These effects boost the MOSFET

electrical performance in relation to the one find in the conventional MOSFET, regarding that they present the same gate area and bias conditions.

III. Experimental Results

In order to understand the advantages and disadvantages of a Diamond MOSFET in comparison to the conventional one counterpart (same gate area and bias conditions), electrical characterizations were performed. These devices were fabricated with 180 nm Bulk CMOS ICs manufacturing process of TSMC.

Regarding that the two devices were submitted to the same bias conditions. Figure 9 shows the curves of drain current (I_{DS}) normalized by the aspect ratio [I_{DS}/(W/L)] as a function of V_{DS} for V_{GS} equal to 0.5V of a DSM and its corresponding Conventional SOI MOSFET counterpart (CSM), regarding that they present the same V_{TNs} (0.29 V).

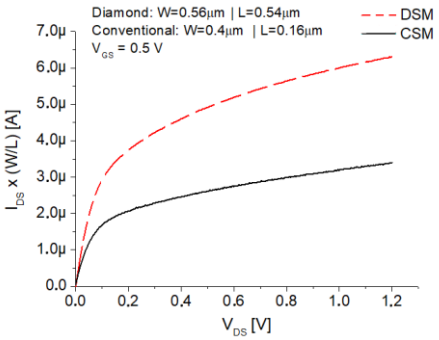

Figure 9: I_{DS}/(W/L) versus V_{DS} curves of CSM and DSM, for V_{GS}=0.5V

Observing Figure 9, we can notice that the Diamond MOSFET I_{DS}/(W/L) is higher than the one found in the conventional counterpart in all operation modes, thanks to the LCE and PAMDLE effects [18]. Besides, regarding V_{DS} equal to 0.8V (saturation region), I_{DS}/(W/L) of the Diamond MOSFET is 53.79% higher than that measured in the conventional counterpart.

The continuation of this work is to implement a new structure for the solar cell considering a base cell defined by the Diamond MOSFET that will be biased by using an external voltage source. After that, three dimensional (3D) numerical simulations will be performed in order to verify the electrical performance of the solar cell implemented with Diamond MOSFETs in relation of that implemented with rectangular MOSFETs.

IV. Conclusion

In order to boost the electrical performance of the solar cells, an innovative structure is been proposed for its implementation which considers the use of Diamond MOSFETs biased. The next step of this work is to create this innovative structure of solar cell in the 3D numerical simulation and perform its electrical characterization. Besides, we will perform a comparative study of this new structure with the typical one, regarding the same areas.

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